UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,902	02/13/2004	Kenneth Koch II	10017912-3	6091

7590 06/12/2007

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
06/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,902	KOCH ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,8,9 and 11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,8,9 and 11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The applicants' amendment submitted on May 11, 2007, and request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. The charging and discharging of a typical capacitor do not fulfill the finite capacitance and open (or the charged and switched off) limitations cited within the present application's independent claims 1, 22, and 26, and as understood by the present examiner with respect to the applicants' arguments and original disclosure.

Amended claim 26 overcame the objections to claims 26 and 27 described in the previous Office Action. Although those objections have been withdrawn, the present examiner has identified another objection, which is described later under the appropriate section.

Also, various claims are now rejected under 35 U.S.C. 112, second paragraph for sections of some claimed limitations the present examiner has deemed to be indefinite, and/or confusing. These rejections are described later under their appropriate section.

After considering the prior art rejections of the previous Office Action, the applicants' arguments/comments, and the original disclosure, all of the prior art rejections described in the previous Office Action have been withdrawn. These include the rejections of: 1) claims 1, 3-4, 8-9, 11, 14, and 22-24 under 35 U.S.C. 102(b), with respect to Ohnishi; and 2) claims 15-19 under 35 U.S.C. 103(a), with respect to Ohnishi/Wanlass/Vikinshi. Ohnishi's capacitors are not considered switchable capacitors by this examiner. Therefore, the previous Office Action's prior art rejections have all been withdrawn to allow the present examiner to reject all the active

claims with respect a different interpretation of the claimed switchable capacitor limitations and known prior art references.

Although page 6 of the previous Office Action indicates claims 26-27 would be allowed, and claims 6, 12-13, 20, 22, and 28-30 were only objected to, those claims are rejected later under 35 U.S.C. 103(a) within this Office Action.

Since new objections and rejections are described below, this Office Action is **NON-FINAL**.

Claim Objections

Claims 19-21 are objected to because of the following informalities: Claim 19, line 3 should have an --and-- added after "inverter," to more clearly separate the first and second resistors' limitations, and to more clearly identify all the intended limitations have been cited within the claim. Dependent claims 20-21 carry over the objection from claim 19. An appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-4, 21, and 26-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear in claim 3 how "a DC power supply terminal" on lines 2-3 relates to claim 1's "opposite power supply terminals" (lines 6-7). For example, is this DC power supply terminal one of the opposite power supply terminals, or another distinct terminal within the circuit? It is believed the finite capacitance values and open circuits within

claim 21, lines 3-7 are reversed. For example, an NFET will not conduct if its control signal is less than the NFET's threshold voltage, but will conduct when the control signal is equal to, or greater than, that threshold voltage. Therefore, won't an NFET configured capacitor have an open circuit when a voltage difference between the gate and source/drain electrodes is below its threshold (thus blocking any charging or discharging operations), and have a finite capacitance when the voltage difference is above that threshold (thus allowing charging and discharging operations)? A PFET configured capacitor will have the opposite effect, wherein it will have a finite capacitance when the voltage difference is greater than the PFET's threshold voltage, but be open when the voltage difference is less than that threshold voltage. Therefore, clarification is requested with respect to the capacitors' finite capacitance values and open circuits as presently recited within claim 21. Claim 26, lines 42-43 "the first transistor (i) is initially off while the first transistor is off" is confusing. For example, was one of these "first" transistors meant to be the "second transistor"? Dependent claims 4 and 27 carry over the rejection from claims 3 and 26, respectively.

Claims 28 and 29 each recites the limitation "the input terminal" in line 10. There is insufficient antecedent basis for this limitation in either claim. For example, what terminal does this "input terminal" actually refer back to?

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-4, 6, 8-9, 11-18, and 22-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma, a reference found during a recent search, in view of Bui et al. (Bui), a reference cited in a PTO-892 previously mailed on Aug 5, 2005. Fig. 1 of Naganuma shows a circuit comprising first terminal 1 understood to be connected to a voltage source (not shown) that provides input signal a transitioning between first/second levels (e.g. 5V and 0V as shown in Figs. 2(A) and 2(B)); driver 7 including first/second opposite conductivity type transistors 71/72 (i.e. PFET 71 and NFET 72) with their respective control electrode b/c, and a (source/drain) path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level (of each transistor); first/second transistor paths of 71/72 are connected in series across opposite power supply terminals 5V and 0V; output terminal 10 is between the paths; circuitry 61,62 is connected between first terminal 1 and control electrodes b/c for causing the first/second transistor paths to be in on and off states (e.g. when the voltage source provides input signal a at a first level (i.e. high), first transistor 71 is on and second transistor 72 is off; and when input signal a is at a second level (i.e. low), first transistor 71 is off and second transistor 72 is on). However, Naganuma does not show or

disclose circuitry 61,62 with at least one voltage responsive switchable capacitor. Bui shows circuitry 802-808 for receiving a single input signal IN and for providing a control signal to driver 809. Bui's circuitry provides a delay period determined by resistive elements 803,805 and capacitive elements 807,808. One of ordinary skill in the art knows this as one type of a time constant circuit. Each of Naganuma's inverter blocks 61 and 62 is also one known type of a time constant circuit (e.g. see column 4, lines 24-27), and Naganuma discloses these time constant circuits suppress output noise and excess current in the driver (e.g. see column 7, lines 62-65), which occurs when both transistors within the driver are conducting at the same time (e.g. see column 2, lines 31-37). Naganuma also discloses that although the simple time constant circuits can be inserted into the circuit, "embodiments are possible to modify in various ways without departing from the spirit of the invention" (e.g. see column 7, lines 62-68). Therefore, it would have been obvious to one of ordinary skill in the art to modify each of Naganuma's inverter blocks 61 and 62 by adding Bui's capacitors 807,808 to the inverter block outputs b/c. With Bui's capacitors 807,808 coupled to output terminals b and c of Naganuma's inverters 61 and 62, respectively, the modified circuit will effectively have the same structure as the applicants' own Fig. 1 with two exceptions (i.e. related to the series connection of a transistor and resistor within each inverter). For example, Naganuma's input terminal 1, first inverter 61 (with PFET 511, NFET 512, resistor R1, and output b), driver 7 (with first (PFET) transistor 71, second (NFET) transistor 72, and output 10), and second inverter 62 (with PFET 521, NFET 522, resistor R2, and output c); and first/second power supply terminals 5V/0V correspond to input terminal 39, first inverter 20 (with PFET 36, NFET 38, resistor 40, and output 28), driver 24 (with first (PFET) transistor 48, second (NFET) transistor 50, and output 26), and second inverter 22 (with

PFET 42, NFET 44, resistor 46, and output 30); and first/second power supply terminals 16/18 shown in the applicants' own Fig. 1. With the addition of Bui's capacitors 807,808 to Naganuma's circuit, NFET 808 (connected to output b) and PFET 807 (connected to output c) correspond to the applicants' NFET 32 and PFET 34, respectively. Therefore, with this circuit configuration, the Naganuma/Bui circuit will be functionally equivalent to the applicants' own Fig. 1, and renders claims 1, 3-4, 6, 8-9, 11-18, and 22-30 obvious. The following descriptions address the claimed limitations in more detail. NFET 808 configured capacitor of Bui will be open when the voltage at its gate (e.g. corresponding to output b or c of its respective inverter block) is below the transistor's threshold voltage, and have a finite capacitance when the voltage at its gate is above the transistor's threshold voltage. Similarly, PFET 807 configured capacitor of Bui will be open when the voltage at its gate (e.g. corresponding to output b or c of its respective inverter block) is above the transistor's threshold voltage, and have a finite capacitance when the voltage at its gate is below the transistor's threshold voltage. Since the threshold voltages of these transistors are between the first and second levels, claim 1 is rendered obvious. The modified Naganuma/Bui circuitry provides a slightly more complex time constant circuit, which can be used to more accurately set the delay time via the RC components within the circuitry. The time constant of each block can be more accurately controlled with this more complex circuitry, thus ensuring that both transistors within driver 7 will not be conducting at the same time (i.e. simultaneously on), and the dead time (i.e. when both transistors are off) will be kept to a minimum. For example, one of ordinary skill in the art knows that excess current caused by both transistors within the driver circuit conducting at the same time is undesirable, and it is preferable to ensure the conducting transistor of the driver will be turned off before the

other transistor within the driver will be turned on. However, too much dead (or blanking) time when both transistors are still off is also undesirable for fast switching operations. Therefore, the on/off operations of the driver transistors must be carefully, and accurately controlled to ensure both transistors are temporarily off before the next transistor begins to conduct, and also to minimize that dead time. This control can be accomplished by utilizing Naganuma's inverter blocks 61 and 62, along with corresponding capacitors from Bui. Since each of power supply terminals 5V and 0V are DC power supply terminals of the circuit, claim 3 is rendered obvious. Resistors R1 and R2, and each transistor within inverters 61 and 62, are resistive type elements, and at least one of them is connected to supply current to their corresponding switchable capacitor in response to the voltage at first terminal 1, rendering claim 4 obvious. First/second transistors 71/72 are PFET/NFET transistors respectively; the opposite power supply terminals 5V/0V are first/second power supply terminals 5V/0V, respectively, wherein first power supply terminal 5V is connected to voltage 5V having a higher value than voltage 0V connected to second power supply terminal 0V; said at least one switchable capacitor 808,807 comprises PFET 807 having a gate electrode connected to gate electrode c of NFET second transistor 72, and source and drain electrodes of PFET capacitor 807 being connected to first power supply terminal 5V, wherein PFET capacitor 807 does not affect current flowing between input terminal 1 and the gate of PFET first transistor 71, rendering claim 28 obvious. Similar to claim 28 described above, but having said at least one switchable capacitor 808,807 comprising NFET 808, it has a gate electrode connected to gate electrode b of PFET first transistor 71, and source and drain electrodes of NFET switchable capacitor 808 being connected to second power supply terminal 0V, wherein NFET capacitor 808 does not affect current flowing between input terminal

1 and the gate of NFET second transistor 72, thus rendering claim 29 obvious. The circuit further comprises another switchable capacitor comprising PFET 807 having a gate electrode connected to gate electrode c of NFET second transistor 72, and source and drain electrodes of PFET capacitor 807 being connected to first power supply terminal 5V, wherein PFET capacitor 807 does not affect current flowing between input terminal 1 and the gate of PFET first transistor 71. This renders claim 30 obvious. Since Naganuma and Bui disclose the relationships between their inventions and integrated circuits (e.g. see column 1, lines 13-15 and column 1, lines 9-11, respectively), it would have been obvious to one of ordinary skill in the art that the at least one switchable capacitor and the PFET/NFET transistors of the driver are included on an integrated circuit chip, and the resistive element (i.e. R1, and/or R2) is a resistor, rendering claim 6 obvious. With a corresponding pair of Bui's switchable capacitors 807,808 coupled to each output of Naganuma's inverter blocks 61 and 62, the at least one switchable capacitor includes first/second voltage controlled switchable capacitors connected to delay coupling of the transitions to the control electrodes of the first/second transistors 71/72, and claim 8 is rendered obvious. For example, the first and second capacitors can correspond to Bui's NFET 808 and PFET 807, respectively. Using NFET 808 connected to control electrode b of first transistor 71, and PFET 807 connected to control electrode c of second transistor 72, as examples, first capacitor 808 will have a finite capacitance on a first side of a first voltage threshold (i.e. above the NFET's threshold), and have a substantially open circuit on a second side of the first voltage threshold (i.e. below the NFET's threshold); and second capacitor 807 will have a finite capacitance on a second side of a second voltage threshold (i.e. below the PFET's threshold), and have a substantially open circuit on a first side of the second voltage threshold (i.e. above the PFET's

threshold). With first capacitor 808 coupled between control electrode b and power supply terminal 0V, and second capacitor 807 coupled between control electrode c and power supply terminal 5V, claim 9 is rendered obvious. Claim 11 is rendered obvious for the same type of reasoning as previously described above with respect to claim 4, and Naganuma's first/second resistive elements R1/R2. First/second transistors 71/72 are PFET/NFET, respectively, and first/second capacitors 808/807 are NFET/PFET, respectively, rendering claim 12 obvious. Similar to claim 6, claim 13 is rendered obvious with the first/second transistors, first/second resistive elements, and first/second capacitors included on an integrated circuit ship, and first/second resistive elements R1/R2 being resistors on the chip. Circuitry 61,62,807,808 further includes first/second inverters 61/62 each having input terminal 1 for simultaneously enabling the first/second inverters in response to voltage at first terminal 1, and an output terminal (b for inverter 61, and c for inverter 62). Output terminal b of first inverter 61 is connected to supply current via a first DC path (through 511) to first capacitor 808 and control electrode b of first transistor 71 to the exclusion of second capacitor 807 connected to control electrode c of second transistor 72; and output terminal c of second inverter 62 is connected to supply current via a second DC path (through 522) to second capacitor 807 and control electrode c of second transistor 72 to the exclusion of first capacitor 808 connected to control electrode b of second transistor 71, rendering claim 14 obvious. Since first/second transistors 71/72, first/second inverters 61/62, and first/second capacitors 808/807 all comprise field effect transistors, claim 15 is rendered obvious. It would have been obvious to one of ordinary skill in the art, as previously described, to include all of the field effect transistors on an integrated circuit chip that includes first/second resistors R1/R2 respectively connected effectively with first/second transistors 71/72

and first/second inverters 61/62, rendering claim 16 obvious. Since first/second resistors R1/R2 are respectively included in first/second inverters 61/62, claim 17 is also rendered obvious. Without repeating the various details previously described above, and since first/second inverters 61/62 each comprise a PFET and an NFET (i.e. inverter 61 comprises PFET 511 and NFET 512, and inverter 62 comprises PFET 521 and NFET 522), and the inverters are driven in parallel by voltage on input terminal 1, claim 18 is rendered obvious. First/second transistors 71/72 are PFET/NFET transistors, respectively, and first/second capacitors 808/807 are NFET/PFET, respectively. First transistor 71 has a source drain path connection to positive power supply terminal 5V, and second transistor 72 has a source drain path connection to negative power supply terminal 0V, wherein these positive/negative power supply terminals are the first/second power supply terminals, respectively. First capacitor 808 has a first electrode connected to gate electrode b of first transistor 71 and a second electrode connected to negative power supply terminal 0V; and second capacitor 807 has a first electrode connected to gate electrode c of second transistor 72 and a second electrode connected to positive power supply terminal 5V. Therefore, claim 25 is rendered obvious. Applying similar reasoning as previously described above, but interpreting the modified configuration described above (i.e. adding Bui's switchable capacitors 807,808 to output terminals b/c of Naganuma's inverters 61/62) in a different manner, during a first interval (e.g. input signal a is high) first transistor 71 will be on and second transistor 72 will be off; and second capacitor 807, connected between 5V and output terminal b, will charge by current flowing from 5V to 0V through 807, 512, and R1, wherein first capacitor 808 (connected to output terminal c) will be off. This will occur because control electrode b (e.g. corresponding to first voltage b) will have a first value (e.g. low), and the 5V coupled to the

other side of second capacitor 807 will allow capacitor 807 to have a finite capacitance and charge, wherein control electrode c (e.g. corresponding to second voltage c) will also have the first value, but since the other side of first capacitor 808 is connected to a low (e.g. 0V), first capacitor 808 will be off. During a second interval (input signal a is low) first transistor 71 will be off and second transistor 72 will be on; and first capacitor 808, connected between 0V and output terminal c, will charge by current flowing from 5V to 0V through R2, 521, and 808, wherein second capacitor 807 (connected to output terminal b) will be off. This will occur because first voltage b will have a second value (e.g. high), and the 5V coupled to the other side of second capacitor 807 will prevent capacitor 807 from charging by switching it off, wherein second voltage c will have the second value, and since the other side of first capacitor 808 is connected to a low (e.g. 0V), second capacitor 808 will have a finite capacitance and be charged. One of ordinary skill in the art would understand that the timing (delay) related to the turning on and off of the first/second transistors will ensure both transistors are never conducting at the same time. However, during the transitioning periods between the first and second intervals, the driver transistor that is initially conducting will be turned off before the other driver transistor will be turned on to minimize excess current (e.g. crowbar or shoot through). As an example, prior to the transition from the first to second interval, the following conditions are present: input signal a is high, first transistor 71 conducts, second transistor 72 is off, first capacitor 808 is off, and second capacitor 807 charges as described above. When input signal a begins to transition from a high to low level, gate electrode b of first transistor 71 will eventually transition low enough to turn off first transistor 71 prior to gate electrode c of second transistor 72 transitioning high enough to turn on second transistor 72. The RC time delay related to inverters 61/62, and

their corresponding capacitors 807,808, will ensure both transistors are temporarily off before second transistor 72 begins to conduct, but with minimal dead time (i.e. when both transistors are off). As input signal a begins to decrease, the current path through 512 and R1 of first inverter 61 turns off and transistor 511 turns on, output terminal b of first inverter 61 becomes high, first capacitor 808 charges, and first transistor 71 turns off. Associated with the high to low transition of input signal a, transistor 522 eventually turns off and the current path through R2 and 521 of second inverter 62 turns on, output terminal c of second inverter 62 becomes high, second capacitor 807 quits charging, and second transistor 72 turns on. Once these conditions are reached, the circuit will be in the second interval. The transition from the second interval to the first interval will be the opposite of those described above. Since one of ordinary skill in the art would understand that these conditions include the charging, discharging, and turning off of the switchable capacitors, claim 22 is rendered obvious. First capacitor 808 will switch off prior to first voltage b reaching the first value (i.e. low), and second capacitor 807 will switch off prior to second voltage c reaching the second value (i.e. high). For example, with first (NFET) capacitor 808 having one electrode coupled to 0V, once the other electrode coupled to first voltage b receives a voltage level less than the threshold of NFET capacitor 808, the capacitor will switch off. This will occur prior to first voltage b eventually decreasing to the first value (i.e. 0V). Similarly, with second (PFET) capacitor 807 having one electrode coupled to 5V, once the other electrode coupled to second voltage c receives a voltage level greater than the threshold of PFET capacitor 807, the capacitor will switch off. This will occur prior to the second voltage c eventually increasing to the second value (i.e. 5V), rendering claim 23 obvious. Since first/second capacitors 808/807 are formed from opposite conductivity transistors, and first

capacitor 808 is connected between first voltage b and 0V, and second capacitor 807 is connected between second voltage c and 5V, the capacitors will be charged and switched off in response to the first/second voltages having values on opposite sides of first/second thresholds respectively associated with the first/second capacitors, thus rendering claim 24 obvious. For example, NFET capacitor 808 has an NFET threshold, and will be off when the voltage at its gate is less than its threshold, wherein PFET capacitor 807 has a PFET threshold, and will be off when the voltage at its gate is greater than its threshold. Claims 26-27 are rendered obvious for the same type of reasoning as described above to the other claims.

Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma/Bui as applied to claim 18 above. As previously described, the obvious modification of Naganuma's circuit with respect to Bui's switchable capacitors, reads on the limitations recited within claim 18, and closely correspond to the applicants' own Fig. 1 circuit. However, the first/second resistors of inverters 61/62 are not connected in the same manner as recited within claim 19 (and shown in the applicants' Fig. 1). However, it would have been obvious to one of ordinary skill in the art to reverse the series connection sequence of Naganuma's first resistor R1 and NFET 512 within inverter 61, and also to reverse the series connection sequence of second resistor R2 and PFET 521 in inverter 62. With these modifications, first resistor R1 will be connected between the source drain path of NFET 512 of first inverter 61 and output terminal b of first inverter 61, and second resistor R2 will be connected between the source drain path of PFET 521 of second inverter 62 and output terminal c of second inverter 62, rendering claim 19 obvious. The positioning of the transistor and resistor within each inverter can be reversed since they are connected in series between the corresponding inverter's output terminal

and the inverter's power supply terminal. Therefore, this series connection forms a current path between those terminals, and since no output is taken from between those two elements (e.g. transistor 512 and first resistor R1), their specific series arrangement is not critical. First/second capacitors 808/807 include NFET 808 and PFET 807, respectively. This renders claim 20 obvious. NFET 808 will have a first (i.e. NFET) threshold, and PFET 808 will have a second (i.e. PFET) threshold, thus they are different, and one of ordinary skill in the art would understand these thresholds are between the first/second levels. First NFET capacitor 808 will have a finite capacitance for a voltage above the first (i.e. NFET) threshold, and have a substantially open circuit for a voltage below the first threshold; and second PFET capacitor 807 will have a finite capacitance for a voltage below the second (i.e. PFET) threshold, and have a substantially open circuit for a voltage above the second threshold. One of ordinary skill in the art would understand the first threshold is greater than the second threshold to ensure the driver transistors will be turned on and off without having both on at any one time, thus rendering claim 21 obvious.

No claim is allowable.

Claims 2, 5, 7, and 10 have been cancelled.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although not used in any prior art references described above, most of these references could obviously be modified to read on at least the basic limitations recited within at least some of the claims. For example, Biesterfeldt (Fig. 1: 110,118,12; 130,138,132; 150; and 152); Dowlatabadi (Fig. 1: 14,18,19; 21,22,30; 36; and 38);

Dijkmans (Fig. 1: 15; 14; P1; and N1); Boomer (Fig. 2: P2,RP,N2,N4; P5,P3,RN,N3; P1; and N1); and Kumagai et al. (Fig. 11: 16,29,17; 23,28,24; 18; and 25) all show circuits that match, or closely correspond to, first inverter 20; second inverter 22; first transistor 48; and second transistor 50, respectively shown in the applicants' own Fig. 1. Hattori (Fig. 1: PFET 27; and NFET 28) and Hanibuchi et al. (Fig. 9: PFETs 70 and 140; and NFETs 80 and 150) each show examples of the use of series coupled PFET/NFET transistors with their common connection being coupled to the output of an inverter, and also to at least one gate of a FET transistor.) Kriz et al. shows NFETs 108,110 utilized as capacitors coupled to the output of a corresponding inverter (103 or 104) in Fig. 1; NFET 210 and PFET 208 utilized as capacitors coupled to the output of a corresponding inverter (204 or 203) in Fig. 2, and also shows/discloses driver 300, 301 having single input IN (see Fig. 3) and drivers (100,101 or 200,201) having complimentary type inputs (e.g. see Figs. 1 and 2). One of ordinary skill in the art understands conventional capacitors can be replaced by FET configured capacitors (e.g. to reduce area), and some of the references also show/disclose this (e.g. see Kikuda et al.: Fig. 3: C1; Fig. 5: C2; and Fig. 7: C3; and Hanibuchi et al.: Fig. 7: 7, 8, 14, and 15; and Fig. 9: 70, 80, 140, and 150). The FET configured capacitors will have finite capacitance and open capabilities, depending on the FET's threshold voltage, and the FET's voltage across their gate and source/drain. Therefore, all of these references should be carefully reviewed and considered with respect to the broadest reasonable interpretation of the claimed invention.

As previously cited above, since this Office Action cites new objections and rejection, it is **NON-FINAL**.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal, can be reached on (571) 272-1769.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

4 June 2007

Kenneth Wells

Kenneth B. Wells
Primary Examiner